SPECIFICATION AMENDMENTS

Amend the paragraph that begins in line 10 on page 2 as follows:

According to the fault simulation method using the logic simulation, however, the fault model that can be simulated is limited only to a single ~~stack-at fault~~ stuck-at fault (Stuck-At-0 or Stuck-At-1) which is a fault that one signal line is stuck at a certain state ("0" or "1"). Therefore, it is impossible with this fault simulation method to simulate, with high sensitivity, a multiple ~~stack-at fault~~ stuck-at fault that plural signal lines are stuck at "0" or "1," a delay fault, a short fault between signal lines, and so on; hence, no lists of detectable faults can be made.

Amend the paragraph that begins in line 3 on page 3 as follows:

An object of the present invention is to provide a fault simulation method and apparatus with which it is possible to make a list of faults detectable by a certain test pattern sequence for delay, open and parameter abnormality faults in semiconductor ICs by the combined use of a transient power supply current, ~~IDDT)~~ IDDQ testing scheme capable of transient phenomena of the ICs and high in observability and the logic simulation.

Amend the paragraph that begins in line 9 on page 6 as follows:

Fig. 1 depicts a transient response of a CMOS inverter. This transient response was obtained with a circuit simulator. As shown in Fig. 1C, the CMOS inverter is formed by a series connection of p- and n-MOS transistors, which is connected at both ends to a power supply terminal T_{VD} and the ground GND. The both transistors have their gates connected to an input terminal IN, and their connection point is connected to an output terminal OUT. Fig. 1A depicts a response of an output voltage V_{OUT} to an input voltage V_{IN} in a transient state, and Fig. 1B depicts a response of a current I_{DD} flowing into the CMOS inverter from the power supply at that time. The current flowing into the CMOS inverter is called a transient current. When the input to the inverter changes from a logic value "1" to "0" as shown in Fig. 1C, the n- and p-MOS transistors simultaneously ~~turns~~ turn ON for a very short period of time when the input voltage V_{IN} is higher than a threshold voltage of the n-MOS transistor but lower than a threshold voltage of the p-MOS transistor, and a short circuit current I_S flows from the power supply terminal T_{VD} to the ground GND. Since at

this time the potential at the output terminal OUT changes from the logic value "0" to "1," a current I_C for charging a parasitic capacitance C_{load} connected to an output signal line (the terminal OUT) of the inverter flows from the power supply terminal T_{VD} at the same time as the short circuit current I_S flows. Accordingly, when the input to the inverter makes a falling transition (described by a suffix "f" to a parameter indicating this state), the transient current I_{Gf} flowing into the inverter is given by the sum of the short circuit current I_{Sf} and the capacitance charging current) I_C as follows:

#3

Amend the paragraph that begins in line 2 on page 10 as follows:

The foregoing description has been given on the assumption that the transient current I_G flowing into the logic gate is mostly the short circuit current I_S. With the recent microfabrication of CMOS circuits, wiring delay becomes dominant over the gate delay. This implies that, assuming that the transition time of the input voltage is fixed, the ratio of the charging current I_C to the output signal line OUT is higher than the ratio of the short circuit current I_S in the transient current I_G that flows into the CMOS logic gate. Hence, the time when the waveform of the transient current I_G of the logic gate reaches its peak is dependent on the ration between the capacitance charging current I_C and the short circuit current I_S. When the capacitance charging current I_C is smaller than the short circuit current I_S, the peak of the waveform of the transient current I_G coincides with the peak of the short circuit current I_S. Since the peak of the short circuit current I_S coincides with the time of transition of the input voltage, the peak of the transient current I_G precedes the transition time of the logic gate output. Conversely, when the capacitance charging current I_C is larger than the short circuit current I_S, the peak of the waveform of the transient current I_G concurs with the peak of the current I_C. Since the capacitance charging current I_C is related to the voltage transition on the output signal line OUT, the peak of the transient current I_G virtually coincides with the transition time of ~~outputting~~ the output from the logic gate.

#4

Amend the paragraph that begins in line 5 on page 14 as follows:

Next, a definition is given of an open fault that leads to the delay fault. The open fault is an unintentional electrical discontinuity, which divides a certain signal line into two or more different signal lines. Included in the open faults are faults such as a break in a contact due to loss of metal or by an oxide film, a break in a metal wire due to patterning

#5

failure or etching failure and a break in a diffusion layer or poly-Si layer due to masking failure. Such open faults fall into two types: an open fault which causes a "logic fault" that the input signal V_{IN} does not ever appear at the output V_{OUT} of a signal line W_i due to an open F_C in the signal line W_i as shown in Fig. 5A, and an open fault which causes a "delay fault" that the input signal V_{IN} passes through the breakage or the portion of the open F_C by, for example, a tunneling current and appears at the output V_{OUT} of the signal line W_i after a time lag as depicted in Fig. 5B. The open fault which causes the logic fault is so large in the scale of open that no current flows even if a voltage is applied to the broken signal line W_i across the breakage. Consequently, the parasitic capacitance is not charged and discharged in association with the signal transition, resulting in the logic fault that logic is kept at a certain value. In contrast thereto, in the open fault which leads to the delay fault, when a voltage is applied to the signal line W_i across the breakage, a very small current is generated; however, since the amount of such current is smaller than the current flow during normal operation, the charge and discharge of the parasitic capacitance associated with the signal transition are delayed, resulting in an increase in the delay time of the circuit. The open faults of this kind are classified into a resistive open fault that the resistance value between signal lines becomes larger than its normal value due to a contact failure or the like or the resistance value of a signal line becomes larger than its normal value due to a failure in the signal line, and a small open fault (< 100 nm) that the tunneling effect generates a very small leak current flow across the breakage. The tunnel current that flows across the small open fault is described, for example, in C. L. Henderson, J. M. Soden, and C. F. Hawkins, "The Behavior and Testing Implications of CMOS IC Logic Gate Open Circuits," Proceedings of IEEE International Test Conference, pp. 302-310, 1991. The present invention is intended for the open fault that causes the delay fault. In this specification the fault of this kind will hereinafter be referred to merely as an open fault.

Amend the paragraph that begins in line 4 on page 40 as follows:

Finally, in step 206 the fault list generating means 103 generates a list of faults detectable by a transient power supply current testing for the test pattern sequences, based on the logic signal value sequences produced in respective signal lines of the IC in the above steps and stored in the memory 102M. When the test pattern sequences are each composed of two test patterns as in the afore-mentioned example, two arbitrary test patterns generated

by the test pattern generating means 102 are taken out and given a test pattern sequence identification number, and the signal lines in which logic signal values change in response to the application of the test patterns are associated, as fault-detectable spots, with the test pattern sequence identification number to make the list of faults. The generation of the fault list will be described in more detail later on. The time series of the logic signal values calculated by the logic simulator 102 for respective test patterns in steps 202, 203 and 204 correspond to the time series of the test patterns in the test pattern sequence.

Amend the paragraph that begins in line 8 on page 46 as follows:

Similarly, in the logic simulation for each internal signal line in the semiconductor IC depicted in Fig. 16, the logic signal values at each input terminal, each internal signal line and each output terminal change in response to the input of each test pattern sequence as depicted in the fig. 17 table. For example, in the case where the set signal propagation path in which a fault possibly occurs is <I3, L3, L5, L12, O2>, the Fig. 17 table shows that I3, L3, L5, L12 and O2 are R, R, R, F and F, respectively for the test pattern sequence T1; that is, the logic signal values change at every point on this signal propagation path. Further, for the test pattern sequence T2, too, I3, L3, L5, L12 and O2 are R, R, R, F and F, respectively; that is, the logic signal values change at every point on this path. Accordingly, the test pattern sequences T1 and T2 are registered in the fault list for the signal propagation path <I3, L3, L5, L12, O2>; alternatively, the path <I3, L3, L5, L12, O2> is registered for each of the test patterns T1 and T2. The signal propagation paths that are registered in the fault list are not limited specifically to the paths from the input to the output terminal of the IC under test but may also be the signal propagation paths that do not reach the output terminal, such as <I1, N1> in the semiconductor IC of Fig. 14 and <I1, L1, L6> in the IC of ~~Fig. 14~~ Fig. 16.

Amend the paragraph that begins in line 17 on page 51 as follows:

Referring to Fig. 23, a description will be given of an example of the procedure for generating a fault list for each signal propagation path in step 906 in Fig. 26. In step 801 one of the signal propagation paths that become possibly faulty in the semiconductor IC under test is initially set. Next, in step 802 it is checked whether the logic signal value sequence at every point in the set signal propagation path, calculated by the logic simulator

102 for the test pattern sequence generated in step 901 in Fig. 26, has been changed. If so, the procedure goes to step 803, then the set signal propagation path is registered in the fault list, and the procedure goes to step 804. For example, in the case where the test pattern T9 in Fig. 15 is generated in step 901in Fig. 26 and the signal propagation path <I1, N1, N3, O1> in the semiconductor IC of Fig. 14 is set in step 801 in Fig. 23, the logic signal value sequence changes at every point in the set signal propagation path, and consequently, the test pattern sequence T9 is registered for the set signal propagation path <I1, N1, N3, O1> in the fault list, or <I1, N1, N3, O1> is registered for T9. The signal propagation paths that are registered in the fault list are not limited specifically to the paths from the input to the output terminal of the IC under test, but signal propagation paths that do not extend to the output terminal from the input terminal, such as <I1, N1> in the semiconductor IC of ~~Fig. 16~~ Fig. 14 and <I1, L1, L6> in Fig. 16 may also be registered. If no logic signal value sequence has been changed at any point in the set signal propagation path, the procedure goes to step 804. In step 804 a check is made to see if there is still left unchecked a signal propagation path that become possibly faulty, and if so, the next signal propagation path that becomes possibly faulty is set in step 805, followed by a return to step 802. In this way, steps 802, 803, 804 and 805 are repeated until all the signal propagation paths that become possibly faulty in the semiconductor IC under test are checked. When no such an unchecked signal propagation path is found, the procedure ends. The processing described above is performed upon each generation of the test pattern in step 901.